(or recess) is disposed within the first gate layer, the gate oxide layer, and the substrate. A field oxide is formed in the trench to a level that is between an upper surface of the substrate and an upper surface of the first gate layer. Preferably, the field oxide level is approximately halfway between the substrate and the first gate layer. An adhesion layer composed of a material other than a conductively doped polysilicon material is formed on the first gate layer. In alternate embodiments, a conductive layer may be formed on the adhesion layer.

In another embodiment, Applicants teach a microelectronic device including a substrate having a trench formed therein, and a field oxide formed within the trench, and a component (*e.g.* a gate structure) formed on the field oxide. The field oxide projects from the trench by a height which is small enough to prevent the formation of spacers adjacent the field oxide. Alternately, the field oxide extends from the trench beyond the surface of the substrate by a height which is less than approximately one half of a height of the component formed on the field oxide.

Because the height of the field oxide "isolation pad" is reduced compared with the height of the gate structure, an edge spacer that may otherwise form along the edges of the isolation pad is reduced or eliminated. Therefore, the isolation pad advantageously requires less surface area on the apparatus.

Manning

Manning teaches trench isolation structures. With reference to Figure 13, Manning teaches structures including a substrate 102, a pad oxide layer 104 on the substrate 102 (4:8-10), a first polysilicon layer 106 on the pad oxide layer 104 (4:18-19), isolation trenches 108, and an oxide layer 112 within each isolation trench "to a thickness which is sufficient to fill isolation trenches 108" (4:54-55). A "conductively doped" second polysilicon layer 116 is formed over the first polysilicon layer 106 (5:16-20). "Second polysilicon layer 114 is conductively doped, since it will form the FET gates." (5:19-20).

Manning does not disclose, teach, or suggest Applicants' disclosed embodiments. For example, Manning does not teach a component (*e.g.* a gate structure) formed on the field oxide isolation pad. Rather, the only components taught by Manning are formed on the substrate.

Manning also does not teach or suggest microelectronic devices having an adhesion layer composed of a material other than a conductively doped polysilicon material

formed on the first gate layer. On the contrary, Manning teaches forming a second polysilicon layer on a first polysilicon layer, the second polysilicon layer being conductively doped to serve as an FET gate. (5:19-20). Furthermore, Manning does not teach or suggest forming a conductive layer over the adhesion layer. Since the second polysilicon layer of Manning is conductively doped, there is no need for a conductive layer formed on an adhesion layer.

<u>Matsumoto *et al*</u>

Submitted herewith is a declaration of inventor Gurtej S. Sandhu under 37 CFR § 1.131 swearing behind Matsumoto *et al* (US 5,726,479). Matsumoto *et al* is therefore removed as prior art. Although Applicants submit that their invention is not anticipated by Matsumoto *et al*, Applicants reserve comment on the merits in view of the enclosed declaration.

I. Rejection of claims 22, 32, and 34-36 under 35 USC § 102(b) as being anticipated by Manning (US 5,177,028).

The Examiner rejected claims 22, 32, and 34-36 under 35 USC § 102(b) as being anticipated by Manning (US 5,177,028). Applicants have amended certain claims to better point out and distinctly claim the subject matter which Applicants regard as their invention. Applicants respectfully request reconsideration of this rejection.

Turning now to the specific language of the claims, claim 22 recites a microelectronic device comprising a microelectronic substrate, a gate structure including a gate oxide layer formed on the substrate, a first gate layer formed on the gate oxide layer, and *an adhesion layer composed of a material other than a conductively doped polysilicon material formed on the first gate layer*, the gate structure having a trench at least partially disposed therein and extending into the substrate, and a field oxide layer at least partially in the trench, the field oxide layer having a field oxide level between the level of an upper surface of the substrate and the level of an upper surface of the first gate layer.

For the reasons set forth above, Manning does not disclose, teach, or suggest a device as recited in Applicants' claim 22. Namely, Manning does not teach or suggest a device having an adhesion layer composed of a material other than a conductively doped polysilicon material formed on the first gate layer.

Similarly, claim 32 recites a microelectronic device comprising a microelectronic substrate having a trench formed in a surface thereof, a gate structure formed on the substrate, the gate structure including a gate oxide layer formed on the microelectronic substrate, a first gate layer formed on the gate oxide layer, *an adhesion layer composed of a material other than a conductively doped polysilicon material formed on the first gate layer, and a conductive layer formed on the adhesion layer*, and a field oxide deposited in the trench, the field oxide extending from the trench beyond the surface of the substrate by a height which is less than or equal to approximately one half of a height of the gate structure formed on the substrate.

Manning does not anticipate a device as recited in Applicants' claim 32 because Manning does not teach or suggest a device having an adhesion layer composed of a material other than a conductively doped polysilicon material formed on the first gate layer. Manning also does not teach or suggest a conductive layer formed on the adhesion layer.

Further, claim 34 recites a microelectronic device comprising a microelectronic substrate having a trench formed therein, a field oxide within the trench and projecting therefrom by a height which is small enough to prevent the formation of spacers adjacent the field oxide, and *a component formed on the field oxide.*

For the reasons set forth above, Manning does not disclose, teach, or suggest a device as recited in Applicants' claim 34. Namely, Manning does not teach a component formed on the field oxide.

Finally, claims 35 and 36 are not anticipated by Manning due to their dependency on claim 22, and also due to additional limitations found in those claims. For example, claim 36 recites a device according to claim 22 wherein the field oxide level is less than or equal to approximately one half the distance between the upper surface of the substrate and the upper surface of the first gate layer. Manning does not disclose, teach or fairly suggest this additional limitation.

For the foregoing reasons, Applicants submit that claims 22, 32, and 34-36 are not anticipated by Manning, and respectfully request reconsideration and withdrawal of this rejection.

II. Rejection of claims 22-37 under 35 USC § 102(e) as being anticipated by Matsumoto et al (US 5,726,479).

The Examiner rejected claims 22-37 under 35 USC § 102(e) as being anticipated by Matsumoto *et al* (US 5,726,479). Submitted herewith is a declaration of inventor Gurtej S. Sandhu under 37 CFR § 1.131 swearing behind Matsumoto *et al* (US 5,726,479). Matsumoto *et al* is therefore removed as prior art. Applicants respectfully request reconsideration and withdrawal of the rejection of claims 22-37 based on Matsumoto *et al*.

III. Rejection of claims 30-31 under 35 USC § 112, second paragraph, as being indefinite.

Applicants have amended claim 30 to remove the indefiniteness caused by the reference to "the trench," which originally lacked antecedent basis. Applicants submit that claims 30 and 31 as amended are now sufficiently definite, and respectfully request the withdrawal of the rejection of these claims.

CONCLUSION

In light of the foregoing amendments and remarks, Applicants believe that claims 22 and 24-37 are in condition for allowance, and that action is respectfully requested.

If there are any remaining matters that can be handled in a telephone conference, Applicants invite the Examiner to phone their attorney, Dale C. Barr, at (206) 903-8745.

Respectfully submitted,
DORSEY & WHITNEY LLP

Dale C. Barr
Registration No. 40,498

DCB/ln
Enclosures:
Postcard
Form PTO-1083 (+ copy)

DORSEY & WHITNEY LLP
U.S. Bank Building Center, Suite 3400
1420 Fifth Avenue
Seattle, Washington 98101
(206) 903-8800
Fax: (206) 903-8820

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